PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Raymond Li
Serial No.: 09/047,320
Filing Date: March 24, 1998
Confirmation No.: 3118
Examiner: Hau H. Nguyen
Art Unit: 2628
Docket No.: 00100.98.1142
Title: **METHOD AND APPARATUS OF VIDEO GRAPHIC AND AUDIO PROCESSING**

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Applicant respectfully submits that the Examiner's rejections include clear errors because the Examiner failed to address claim language, one or more claim limitations are not taught by the cited references and the references do not teach what the Examiner alleges.

Claims 1-3 and 6-23 stand rejected under 35 U.S.C. Section 102(e) as being anticipated by Swanstrom, et al. As such, Swanstrom alone must describe each and every limitation as actually claimed.

As to claim 14, the office action failed to address the claim language of this claim and instead rejected the claim in its entirety stating "Claims 6-23, which are similar in scope to claims 1-3, are thus rejected under the same rationale." (Office action, page 3). Applicant repeatedly requested a properly detailed rejection in numerous responses but received none. Applicant respectfully submits that claim 14 includes, for example, a processing unit and memory that contains executable instructions that when executed, cause the processing unit to receive at least one address in an associated data command and audio process the associated data command when the address identifies audio processing and graphics process the associated data command when the address identifies graphics processing. No such processing unit has been identified by the Examiner to be in Swanstrom nor has any memory containing executable instructions containing the executable code as claimed been identified by the office action and as such, Applicant respectfully submits that there has not been a prima facia showing of an

anticipation under the rules of the U.S. Patent Office and as such, the Examiner has committed clear error.

In addition, language of claims 8-11 have also not been addressed. For example, claims 8 and 9, were summarily rejected without any basis or reasoning as allegedly having the same scope of claims 1-3. However, claims 8 and 9 refer to enabling audio processing circuit to receive incoming data via a local bus wherein at least one address identified the audio processing circuit and when the associated command is for inputting data. This claim language was not addressed. As such, the Examiner made a clear error. As to claim 9, a claim which depends on claim 7, the claim requires enabling the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting data. Other claims including claims 10 and 11 were similarly overlooked and no reasoning has been provided nor any portion of any referenced cited as allegedly teaching the subject matter of these claims in the office actions. Accordingly, Applicant respectfully submits that the Examiner has committed clear error.

As to claim 1, it appears that claim language is being overlooked and that different elements from different embodiments appear to be combined in the rejection in an attempt to render the claim anticipated. For example, the office action alleges that arbiter 504 FIG. 7 (or 614 of FIG. 10) correspond to the claimed bus arbiter. It is noted that FIGs. 7 and 10 refer to a different embodiment from other embodiments described in the reference and in particular, the arbiters 504 and 614 are connected with a "control channel". The control channel as described in Swanstrom is used so that the PCI bus 120 (alleged to correspond to the claimed system bus) is not used. As stated in column 14:

> When the multimedia devices 142A-146A communicate using the real-time bus 130, the devices use the control channel 502 for addressing, control, status and handshaking signals. Thus the devices 142A-146A do not utilize any PCI bus cycles when communicating over the multimedia bus 130. (column 14, lines 29-34). (Emphasis added).

As such, the alleged "system bus" – the PCI bus 120 – in Swanstrom is not used when the arbiter 504 is used. The arbiter 504 is connected to the control channel for addressing signals, control and status signals. Applicant respectfully submits that the arbiter 504 of FIG. 7 and the configuration shown in FIG. 7 or FIG. 10 as indicated above teaches that the alleged system bus is not used during the arbitration operation. As further described in column 13, FIG. 7 shows a dedicated control channel 502 that is separate from the PCI bus 120 and the multimedia bus 130 for transferring control information for the multimedia bus data transfers. The multimedia data transfer initially involves the transfer of control information on the dedicated control channel 502 which includes the arbiter 504, followed by the transfer of data streams preferably periodic data streams on the multimedia bus 130. When employing the arbiter 504 and separate control bus 502 and using the real time bus 130, the system bus 120 is not utilized.

This is different from the claimed circuit. The claimed bus arbiter, alleged to be arbiter 504 for example, "interprets the incoming data" from the system bus and provides the incoming data from the system bus to the audio processing circuit or the video graphics processing circuit. Such a bus arbiter is not described in the cited portions because the bus arbiter 504 does not interpret incoming data on the system bus – alleged to be PCI bus 120 – since PCI bus 120 as described in column 14 is not utilized. As such, Applicant respectfully submits that the reference does not teach the claimed subject matter and the rejection must be withdrawn.

In addition, Applicant notes that the claim is directed to a circuit that includes both a graphics processing circuit, an audio processing circuit and bus arbiter as claimed. The Swanstrom reference does not describe such circuits coupled to an arbiter but instead describes whole "devices" being connected through a dedicated multimedia bus. Since the reference does not teach the claimed subject matter, the rejection must be withdrawn.

As to claim 2, the claim requires that the bus arbiter routes received data to the graphics processing circuitry when the address is received via the local bus to route received data to the audio processing circuit when the address identifies the audio processing circuit. Applicant respectfully submits that the arbiter of Swanstrom does not route data but instead merely allows one "device" to be accessing the dedicated bus at a time. The "Response to Arguments" section attempted to address this apparently by referring to FIG. 3A of Swanstrom, column 9, lines 35-59. However, the cited portion does not refer to the operation that employs the arbiter of FIG. 7. To the contrary, it refers to the embodiment where no arbiter 504 is being employed. Moreover, the cited portion in addition to not referring to the bus arbiter as required by the claim, also merely indicates that an address indicating a destination address is transferred along with control information to another device. This operation is not being claimed by Applicant. Accordingly, Applicant respectfully submits that there was clear error with respect to claim 2.

As to claim 6, Applicant respectfully notes that the claim requires among other things, a method for bus arbitration among an audio processing circuit and a graphics processing circuit which includes determining whether at least one address identifies at least one of the audio processing circuit or the graphics processing circuit and when the address identifies both, arbitrating access to a local but between the two circuits. There is no portion in the sited reference set forth in the office action that addresses this claim language. In addition, since the address as claimed identifies both processing circuits, Applicant respectfully requests a showing as to which cited portion of the reference anticipates the subject matter in addition to the arbitration operations has if the rejection is unauthorized, claimed as applicant is unable to find such a teaching.

Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Swanstrom et al. in view of Post. Applicant respectfully reasserts the relevant remarks made above and as such these claims are also in condition for allowance.

Claim 24 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Swanstrom. This is an anticipation rejection. However, the final action states that "it would have been obvious to one skilled in the art" to integrate all the components into a single chip. Applicant respectfully submits that the rejection is an improper anticipation rejection and therefore the rejection must be withdrawn.

Moreover, Applicant respectfully challenges the conclusion since Swanstrom specifically teaches "separate devices" which is a similar type of prior art system noted in Applicant's Background of the Invention section. Such systems require multiple video graphic circuit boards or audio processing circuit boards and do not utilize or require the claimed structure. In addition, Applicant respectfully notes that claim 24 is also at least allowable as depending from an allowable base claim. As noted above, no bus arbiter is claimed in combination with the circuits that are provided in the cited references.

Withdrawal of the rejections of the claims is respectfully requested and a Notice of Allowance is respectfully requested.

Respectfully submitted,

Date: February 6, 2008

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